Patent claims

1. A component, with a connection, as well as at least one further connection, in which differential input clock pulses can be applied to the connections, or a single input clock pulse can be applied to the connection and/or to the further connection wherein the component further comprises a first and a second pulse relay device, whereby the first pulse relay device is arranged for relaying differential input clock pulses, and the second pulse relay device for relaying a single input clock pulse.

2. A component according to claim 1, in which the first pulse relay device is specially arranged for relaying differential input clock pulses, and/or the second pulse relay device is specially arranged for relaying a single - input - clock pulse.

3. A component according to claim 1, in which the second pulse relay device then induces the emission of a differential output clock pulse on a corresponding pair of lines, when it is detected that there is a single input clock pulse present at connection and/or at the further connection.

4. A component according to claim 3, which also contains a circuit device to detect whether differential input clock pulses are present at the connections, or a single – input - clock pulse at connection and/or at the further connection.

5. A component according to claim 4, whereby the circuit device determines whether an input - clock pulse is present at the connection and/or at the further connection, in order to determine whether differential input clock pulses are present at the connections, or whether a single - input - clock pulse is present at the connection and/or at the further connection.

6. A component according to claim 5, in which the circuit device contains a comparison device for comparing signals present at the connection, more particularly input - clock pulses, with a reference signal.

7. A component according to claim 6, in which the comparison device contains a differential amplifier.

8. A component according to claim 7, in which the comparison device then emits an impulse, more particularly an - input - clock pulse detection signal, when the level of the signal present at the connection exceeds or falls below a predetermined level, more particularly the level of the reference signal.

9. A component according to claim 8, with which an impulse, more particularly an input clock pulse detection signal is then emitted by the comparison device when the level of the signal present at connection first exceeds a predetermined initial level, and then falls below a predetermined second level that differs from the initial level.

10. A component according to claim 8, with which an impulse, more particularly an input clock pulse detection signal is then emitted by the comparison device, when that level of the signal present at connection first falls below a predetermined initial level, and then exceeds a predetermined, second level that differs from the initial level.

11. A component according to claim 10, which furthermore contains a counter device, particularly for detecting the number of impulse, more particularly input clock pulse detection signals emitted by the comparison device.

12. A component according to claim 11, with which it is determined that an input clock pulse is present at connection, when the number of impulses, more particularly input clock pulse detection signals emitted by the comparison device and detected by the counter device, is larger than or equal to a predetermined number.

13. A component according to claim 11, wherein the component is a DDR semi-conductor component, more particularly a DDR semi-conductor memory component.

14. A component according to claim 13, in which the memory component is a DRAM (Dynamic Random Access Memory).

15. A component according to claim 2, in which the second pulse relay device then induces the emission of a differential output clock pulse on a corresponding pair of lines, when it is detected that there is a single input clock pulse present at connection and/or at the further connection.

16. A component according to claim 15, which furthermore contains a counter device, particularly for detecting the number of impulse, more particularly input clock pulse detection signals emitted by the comparison device.

17. A component according to claim 16, with which it is determined that an input clock pulse is present at connection, when the number of impulses, more particularly input clock pulse detection signals emitted by the comparison device and detected by the counter device, is larger than or equal to a predetermined number.

18. A component according to claim 15, which also contains a circuit device to detect whether differential input clock pulses are present at the connections, or a single – input - clock pulse at connection and/or at the further connection.

19. A component according to claim 1, which furthermore contains a counter device, particularly for detecting the number of impulse, more particularly input clock pulse detection signals emitted by the comparison device.

20. A component according to claim 13, wherein the component is a DDR semi-conductor component, more particularly a DDR semi-conductor memory component.